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Description

[METHOD FOR REDUCING AMINE BASED CONTAMINANTS]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This Application claims priority to U.S. provisional application serial no. 60/429,828, filed on November 27, 2002, which is incorporated herein in its entirety.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] The invention generally relates a semiconductor device and method of manufacture and, more particularly, to a semiconductor device and method of manufacture which reduces the occurrence of resist poisoning.

[0004] Background Description

[0005] To fabricate microelectronic semiconductor devices such as an integrated circuit (IC), many different layers of metal and insulation are selectively deposited on a silicon wafer. The insulation layers may be, for example, silicon dioxide,

silicon oxynitride, fluorinated silicate glass (FSG), carbon doped, silicon dioxide or organosilicad glass (OSG) and the like. These insulation layers are deposited between the metal layers, i.e., intermetal dielectric (IMD) layers, and may act as electrical insulation therebetween or serve other known functions. These layers are typically deposited by any well known method such as, for example, plasma enhanced chemical vapor deposition (PECVD), chemical vapor deposition (CVD) or other processes.

[0006] The metal layers are interconnected by metallization through vias etched in the intervening insulation layers. To accomplish this, the stacked layers of metal and insulation undergo photolithographic processing to provide a pattern consistent with a predetermined IC design. By way of example, the top layer may be covered with a photo resist layer of photo-reactive polymeric material for patterning via a mask. A photolithographic process using either visible or ultraviolet light is then directed through the mask onto the photo resist layer to expose it in the mask pattern. An antireflective coating (ARC) layer such as PECVD SiON or spin on coating materials may be provided at the top portion of the wafer substrate to minimize reflection of light back to the photo resist layer for more

uniform processing. The spin on ARCs may include AR-14™ (manufactured by Shipley Company, LLC of Marlborough, MA) or sacrificial light absorbing material (hereinafter referred generally as SLAM).

[0007] To form vias, for example, etching may be used to connect the metal layers deposited above and below the insulation or dielectric layers. The etching may be performed by anisotropic or isotropic etching as well as wet or dry etching, i.e., RIE (reactive ion etching), depending on the physical and chemical characteristics of the materials. To maximize the integration of the device components in very large scale integration (VLSI), it is necessary to increase the density of the components. This requires very strict tolerances in the etching and photolithographic processes.

[0008] However, it is known that resist poisoning can occur during the photolithographic processes. One example of resist poisoning during the lithographic process is caused by amine-induced poisoning of chemically amplified resists created during the patterning step. This may be caused when low k dielectrics are used for the IMD and interlevel dielectric (ILD). In a more general example, during the photolithographic process, contaminants that are

incompatible with the photo-reactive polymeric material can migrate into the photo resist layer from the deposited film on the wafer, itself. These contaminants then poison the photo resist layer, which may result in a non-uniformity of the reaction by extraneous chemical interaction with the polymeric material. The resist poisoning also may result in poor resist sidewall profiles, resist scumming and large CD variations. This leads to the formation of a photo resist footing or pinching, depending on whether a positive negative or photo resist, respectively, is used during the process. This may also lead to an imperfect transfer of the photo resist pattern to the underlying layer or layers thus limiting the minimum spatial resolution of the IC.

[0009] One known method to solving this problem is to run a totally free nitrogen or nitrogen containing molecule free process. Examples of nitrogen containing molecules include N_2, NH_3, NO, NO_2, etc. However, all released FSG films are known to require either N_2O (silane films) or N_2 (TEOS) films. In addition, silicon nitride or silicon carbon nitride is commonly employed as a copper cap under the IMD due to its superior electromigration performance as compared to silicon carbide. Finally, even if totally nitro-

gen free films are used, nitrogen from the ambient air, ARC/photoresist or nitrogen impurities contained in the deposition or etch gases can result in the presence of amines.

SUMMARY OF INVENTION

[0010] In a first aspect of the invention, a method for reducing resist poisoning is provided. The method includes forming a first structure such as, for example, a trench or via in a dielectric on a substrate and reducing amine related contaminants from the dielectric and the substrate created after the formation of the first structure. The method further includes forming a second structure in the dielectric.

[0011] In another aspect of the invention, the first structure such as, for example, a trench or via in a dielectric on a substrate. A first organic film is formed on the substrate which is then heated and removed from the substrate. A second organic film is formed on the substrate and patterned to define a second structure in the dielectric.

[0012] In yet another aspect of the invention, a method for reducing resist poisoning includes forming a first structure such as, for example, a trench or via in a dielectric on a substrate and performing DHF wet etch with an approximate ratio of 100:1 on the dielectric. An anti-reflective

coating (ARC) is formed on and then removed from the dielectric and the substrate. A second organic film is then formed on the substrate and patterning of the second organic film is performed to define a second structure in the dielectric.

[0013] In still another aspect of the invention, the first structure is formed in a dielectric on a substrate. A wet etching is provided on the formed first structure at approximately 3nm 100:1 ratio of DHF. An organic film is applied on the exposed portions of the first structure, the dielectric and the substrate. The applying step includes spin coating of the organic film on the exposed portions, baking the organic film at approximately 100 degrees Celsius to 250 degrees Celsius and removing the organic film by dry stripping or plasma etching. The structure thus formed is then capped and a second organic film is formed on the substrate and patterned to define a second structure in the dielectric.

[0014] In an aspect of the invention, the structure is embedded in the dielectric with a vertical dielectric adjacent to a vertical sidewall of the structure. The vertical dielectric is deposited after the patterning and etching of a structure into the dielectric. The dielectric includes one of SiO_2, F-doped

SiO_2, and CH_3-doped SiO_2. The vertical dielectric includes one of SiO_2, P-doped SiO_2, F-doped SiO_2, B-doped SiO_2, and B- and P-doped SiO_2.

Brief Description of Drawings

[0015] Figures 1a through 1e represent a typical fabrication technique for forming a layered structure using standard reactive ion etching (RIE) technique;

[0016] Figure 2 represents a first aspect of the invention;

[0017] Figures 3a through 3c represent another aspect of the invention;

[0018] Figures 4a through 4d represent another aspect of the invention;

[0019] Figures 5a through 5d show a trough lithographic process after contaminants are constrained, bound or capped in lower layers;

[0020] Figure 6a is a representation of a top view of a device using the methods of the invention;

[0021] Figure 6b is a representation of a cross sectional side view of a device using methods of the invention; and

[0022] Figure 7 shows an embodiment of the structure of the invention.

Detailed Description

[0023] This invention is directed to a semiconductor device and method of manufacture and, more particularly, to a semiconductor device and method of manufacture which reduces the occurrence of resist poisoning in the device. By reducing poisoning effects, the invention also significantly reduces photo resist footing or pinching, depending on the use of a positive negative or photo resist, respectively. The reduction of the poisoning allows for the fabrication of more densely packed integrated circuits (IC) with better resolution of interconnects and the like thereon. This, in turn, results in a superior performance of the IC. The formation of vias and troughs can be characterized as either a first structure or a second structure, depending on the architecture of the device.

[0024] Figures 1a through 1e represent a typical fabrication technique for forming a layered structure using standard reactive ion etching (RIE) technique. The RIE process should be well understood by those of ordinary skill in the art and is not discussed in great detail herein. In the schematics, a multilayer arrangement on a semiconductor substrate, which is typically a silicon substrate, is shown. The substrate may equally represent any type of film having known contaminants such as amines, for example.

[0025] Figure 1a shows a target layer 12 such as an oxide layer deposited on the substrate 10. In one embodiment, the oxide layer is approximately 8000 Å. Any known photo-resist or ARC/photo-resist 14 is then deposited on the oxide layer. Figure 1b represents a photolithographic process performed on the photo-resist layer 14. In this representation, the photo-resist layer 14 is exposed to light through a mask 16 to form an image on the photo-resist layer 14. Once the exposure is complete, the exposed photo-resist layer 14 is developed in order to remove those portions of the exposed photo-resist. This is typically performed by a wet develop process using, for example, TMAH, as known in the art. The resulting pattern is shown in Figure 1c.

[0026] A reactive ion etching is then performed on the target layer 12 in order to form a first structure such as a via 16, for example (Figure 1d). The first structure may equally be a wire trough, in some applications. The remaining portions of the photo-resist layer 14 are then removed by, for example, dry strip techniques (Figure 1e) using, for example, $O_{2,}$ H_2, N_2, plasmas or damascene plasmas, all known in the art. In one embodiment, the first structure (i.e., a via) is at a depth of about 7500Å. It should be well

understood by those of ordinary skill in the art, though, that other depths are also contemplated by the invention. At the end of this process, contaminants are known to be associated with the substrate 10 or target layer 12 basically due to the etching process, to this stage.

[0027] Figure 2 is representative of a first embodiment of the invention. In Figure 2, the structure of Figure 1e is subjected to a plasma wafer treatment. In one embodiment, the plasma wafer treatment is an N_2O plasma treatment performed at approximately 400 degrees Celsius. In one aspect, the N_2O will chemically tie up the contaminants such that the contaminants will not diffuse out from either the substrate layer 10 or the target layer 12, i.e., oxide layer. In another aspect, it is assumed that the N_2O passivates the exposed layer in order to bind, trap or consume the contaminants such that amine, for example, will not diffuse out from the exposed layers during subsequent etching processes. In either scenario, it is known that the plasma wafer treatment of the invention prevents poisoning of the resist layer in subsequent processing steps. An alternative embodiment uses a N_2O, O_2 or H_2 plasma with no deposition in order to achieve the same effect. The time for the N_2O, O_2 or H_2 plasma may be from one to 60

seconds, for example, alternative, the wafer may be baked for approximately 0.1 to 10 minutes at 400 degrees Celsius to partially outgas amines.

[0028] Figures 3a through 3c represent another aspect of the invention. In Figure 3a, an optional wet etching of approximately 30 seconds at 25 degrees Celsius, 100:1 ratio of DHF (dilute hydrofluoric acid) is performed on the device of Figure 1e. It should be recognized by those of ordinary skill in the art that other ratios, times or temperatures of the DHF may also be used in accordance with the principles of the invention. In Figure 3b, an organic film such as an antireflective coating 18 (ARC) is applied to the device of Figure 1e, with or without the optional wet etching being performed. In one aspect, the ARC is spin coated onto the entire exposed surfaces of the target layer 12 and the substrate 10. The ARC is then baked at approximately 100 degrees Celsius to 250 degrees Celsius and more preferably between 150 degrees Celsius to 220 degrees Celsius in order to diffuse the amine based contaminants into the ARC. The ARC is removed by dry stripping or plasma etching, similar to that described above with reference to the photo-resist layer 14. This latter step is shown in Figure 3c. The ARC may be exposed to UV light.

[0029] Figures 4a through 4d represent another aspect of the invention. Figures 4a through 4c are substantially identical to those steps shown and described with reference to Figures 3a through 3c, and are not described again. Figure 4d shows the deposition of a thin plasma cap 20. The cap 20 can be deposited by any known method such as, for example, PECVD, HDPCVD, SACVD, APCVD and the like at a temperature ranging from 25 degrees Celsius to 500 degrees Celsius, and preferably at 400 degrees Celsius. In one aspect, the oxide cap 20 is approximately 25 nm; however, other thicknesses are also contemplated for implementation by the invention. In one embodiment, prior to the deposition of the oxide cap, an annealing process is performed at about 400 degrees Celsius for about 60 seconds. In another embodiment, prior to the deposition of the oxide layer, a N_2O or O_2 plasma etch at an approximate temperature of 400 degrees Celsius is performed. (These steps may be represented by Figure 4c.) The silicon dioxide cap will seal any of the remaining amine based contaminants in the layers 10 and 12. In the process described with reference to Figures 4a-dc, any amine based contaminants will not diffuse out during subsequent processing steps to contaminate the resulting device.

[0030] Figures 5a through 5d show a typical trough lithographic process after the contaminants such as, for example, amine based contaminants, are constrained, bound or capped in the lower layers 10 and 12. This process will now provide a second structure such as channels or troughs in the target layer 12, but without any contaminants from the resist or other device layers contaminating the device during this further processing stage. In another aspect, the second structure may be a via. In accordance with the invention, more accurate troughs can be achieved, increasing the density of the device in addition to its performance.

[0031] In particular, Figure 5a shows a known photo-resist 20 deposited on the oxide layer 12. Figure 5b represents a photolithographic process performed on the photo-resist layer 20. In this representation, the photo-resist layer 20 is exposed to light through a mask 22 to form channels or troughs in the photo-resist layer 20. Once the exposure is complete, the exposed photo-resist layer 20 is developed in order to remove those portions of the exposed photo-resist. The resulting pattern is shown in Figure 5c. A reactive ion etching is then performed on the target layer 12 in order to form one or more channels 24, for example

(Figure 5d). The remaining portions of the photo-resist layer 18 are then removed by, for example, dry strip techniques (Figure 5d) to form the channels "C"of the final device structure.

[0032] It should be understood that the steps shown in Figure 2, Figures 3a through 3c or Figures 4a through 4d may be repeated if other structures are to be formed on any overlaying layers. Likewise, in any multilayered structure, the steps shown and described herein may be repeated to reduce or eliminate contaminants during further processing. This is mainly due to the fact that more contaminants may have formed on or diffused into the layers, now shown, or additionally formed layers due to the use of additional resist layers and etching or other processing steps.

[0033] Table 1, reproduced below, is representative of the advantages achieved by the aspects of the invention, compared to conventional methods. The date in Table 1 and table 2 were generated using duel damascene wires and vias with 200nm minimum critical dimension. In Table 1, it is shown that a conventional method of fabrication yields approximately 15% non-defective devices (chips). In stark improvement, the use of the aspect of Figure 2 shows a yield of 60% of non-defective devices (chips). Of

even greater yield is the aspect of the invention of Figures 3a through 3d which show a yield of 75% of non-defective devices (chips). The aspect of the invention of Figures 4a through 4d shows a yield of 90% of non-defective devices (chips). This improvement over the standard fabrication processes is attributable to the elimination of contaminants during the fabrication processes.

[0034]

TABLE 1

Process	#lots	% chips with greater than 0 resist poisoning defect yield
Standard process	6	15%
Added lithographic work	24	60%
Added DHF clean and lithographic work	38	75%
Added DHF clean + litho work +thin oxide cap	50	90%

[0035] Table 2 represents the critical dimension (CD) or diameter of the via using either a 40 mJ or 70 mJ dose. As seen in Table 2, below, the standard fabrication process, at 40 mJ, provides an approximate via size of 200 nm with "scummed" edges. That is, the edges of the via using the standard fabrication process has resist that does not completely clear out thus resulting in blurred edges. In stark contrast, the aspects of the invention result in vias with clearly defined edges. Additionally, the via are also larger due to the suppression of the poisoning.

[0036]

TABLE 2

Process	Via 40mJ dose	Via cd 70 mJ dose
Standard	Scummed approx. 200nm	360 nm
400C oxygen plasma	400 nm	____
DHF + thin oxide cap	400 nm	500 nm

[0037] In one embodiment, the formation of the via on the target layer is a first structure and the formation of the trough is a second structure. The first and second structure, however, can be switched, depending on the design of the device. In one aspect, the dimension of the first structure is about 200 nm and the photolithographic exposure wavelength is about 248 nm. Of course, those of ordinary skill in the art will readily recognize that other dimensions and photographic minimums are also contemplated by the invention and that the above example is only one illustrative embodiment of the invention.

[0038] Figure 6a shows a top view of an example of the device of the invention with both a first structure and a second structure. Figure 6b shows a cross sectional view of an example of the device of the invention. The views of Figures 6a and 6b are taken in a scanning electron microscope of a dual damascene copper wire and via with resist poisoning.

[0039] It is contemplated by the invention that the SiO_2 thin oxide cap can be a sacrificial film (i.e., it is removed during

the post via RIE clean, trough RIE, post trough RIE clean, or other steps). Alternatively, the SiO_2 thin oxide cap can remain on the wafer post-metallization, as shown in Figure 7, layer 7, for example. More particularly, Figure 7 shows dual damascene wire 2 and via 3 contacting the previous metal level 4. The wire 2 and via 3 are embedded in dielectric 1 and the wire 4 is embedded in dielectric 6. An optional via RIE stop layer or copper diffusion barrier 5 is deposited over dielectric layer 6 and wire 4. If the SiO_2 thin oxide cap is not removed during processing, then it will remain on the wafer as shown by layer 7.

[0040] In an aspect of the invention, the structure is embedded in the dielectric with a vertical dielectric adjacent to a vertical sidewall of the structure. The vertical dielectric is deposited after the patterning and etching of a structure into the dielectric. The dielectric includes one of SiO_2, F-doped SiO_2, and CH_3-doped SiO_2. The vertical dielectric includes one of SiO_2, P-doped SiO_2, F-doped SiO_2, B-doped SiO_2, and B- and P-doped SiO_2.

[0041] While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modifications and in the spirit and scope of the appended claims.